Appl. No. 10/604,268
Amdt. dated September 30, 2005
Reply to Office action of June 30, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

5   ## Listing of Claims:

Claim 1 (Original): A computer system, the computer system comprising:

     a processor for controlling operations of the computer system;

     a dynamic random access memory (DRAM) electrically connected to the processor for storing data;

10   a south bridge chipset electrically connected to the processor and the DRAM, the south bridge chipset comprising:

         a system controller for controlling operations of the south bridge chipset;

         a buffer for temporarily storing the data;

         a memory controller for accessing the data in the DRAM;

15   an integrated device electronics controller (IDE controller) for accessing data in an integrated device electronics (IDE) component; and

         a data conversion circuit electrically connected to the memory controller and the IDE controller for converting a hard-disk access command transmitted from the system controller to the IDE controller into a memory access

20   command of the memory controller wherein the memory controller accesses the buffer and the DRAM by executing the memory access command;

     a power supply for generating a plurality of operating voltages to drive the computer system; and

25   a battery device for generating the operating voltages that self-refresh the DRAM;

36

Appl. No. 10/604,268
Amdt. dated September 30, 2005
Reply to Office action of June 30, 2005

wherein when the computer system performs a power supply management operation consistent with an advanced mode and an advanced configuration and power interface (ACPI) and enters a power-saving mode, the computer system can make use of the battery device to constantly self-refresh the DRAM for maintaining
5   the data stored in the DRAM.

Claim 2 (Currently Amended): The computer system of claim 1 further comprising a switch electrically connected to the battery device wherein when the computer system enters the power-saving mode, the power supply ceases providing the
10   operating voltage for self-refreshing the DRAM, and the switch will be enabled to make the battery device provide the operating voltage for self-refreshing the DRAM, wherein the power-saving mode comprises [[a]] an S4 status and [[a]] an S5 status.

Claim 3 (Original): The computer system of claim 1, wherein the battery device is a
15   rechargeable battery.

Claim 4 (Original): The computer system of claim 1, wherein when the computer system is powered-on, the power supply will provide the operating voltage for refreshing the DRAM and the switch will be disabled, and then the power supply will charge the
20   battery device.

Claim 5 (Currently Amended): The computer system of claim 1, wherein the memory controller accesses an input data temporally temporarily stored in the buffer of the south bridge chipset according to the memory access command, and the input data
25   will be stored in the DRAM.

Claim 6 (Original): The computer system of claim 1, wherein the memory controller accesses an output data in the DRAM according to the memory access command,

37

and the output data will be stored in the buffer of the south bridge chipset.

Claim 7 (Original): The computer system of claim 1 further comprising a basic
input/output system (BIOS) for executing a power on self test (POST) of the
5   computer system, wherein the BIOS executes the POST and divides the DRAM into
a first memory section and a second memory section, and the second memory
section is set as a memory capacity that can be used for the operating system of the
computer system and the first memory section can be accessed by the memory
access command corresponding to the hard-disk access command.

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Claim 8 (Original): The computer system of claim 7, wherein the DRAM comprises at
least two memory modules installed in two memory slots of the computer system
respectively, and one of the memory modules corresponds to a first memory section
and the other memory module corresponds to a second memory section.

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Claim 9 (Original): The computer system of claim 8, wherein the DRAM comprises a
memory module installed in a memory slot of the computer system.

Claim 10 (Original): A method for storing data in a computer system, the computer
20   system comprising a processor for controlling operations of the computer system, a
dynamic random access memory (DRAM) electrically connected to the processor for
storing the data, a south bridge chipset electrically connected to the processor and
the DRAM for converting a hard-disk access command into a memory access
command and for executing the memory access command corresponding to the
25   hard-disk access command to access the DRAM, a power supply for generating a
plurality of operating voltages to drive the computer system, and a battery device for
providing the operating voltage that self-refreshes the DRAM, the method
comprising:

38

providing the battery device to constantly self-refresh the DRAM for maintaining the data stored in the DRAM when the computer system performs a power supply management operation consistent with an advanced mode and an advanced configuration and power interface (ACPI) and enters a
5   power-saving mode.

Claim 11 (Original): The method of claim 10, wherein the battery device is a rechargeable battery.

10   Claim 12 (Original): The method of claim 11, wherein when the computer system is powered-on, the power supply will provide the operating voltage for refreshing the DRAM and a switch will be disabled, and then the power supply will charge the battery device.

15   Claim 13 (Currently Amended): The method of claim 10, wherein the power-saving mode comprises [[a]] an S4 status.

Claim 14 (Currently Amended): The method of claim 10, wherein the power-saving mode comprises [[a]] an S5 status.
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Claim 15 (Original): The method of claim 10, wherein the memory controller accesses an output data in the DRAM according to the memory access command, and the output data will be stored in the buffer of the south bridge chipset.

25   Claim 16 (Original): The method of claim 10, wherein the computer system further comprises a basic input/output system (BIOS) for executing a power on self test (POST) of the computer system, the method further comprising:
       executing the POST and dividing the DRAM into a first memory section and a

39

Appl. No. 10/604,268
Amdt. dated September 30, 2005
Reply to Office action of June 30, 2005

second memory section; and

setting the second memory section as a memory capacity that can be used for the operating system of the computer system;

wherein the first memory section can be accessed by the memory access command
5 corresponding to the hard-disk access command.

Claim 17 (Original): The method of claim 16, wherein the DRAM comprises at least two memory modules respectively installed in two memory slots of the computer system, and one of the memory modules corresponds to the first memory section and the
10 other memory module corresponds to the second memory section.

Claim 18 (Original): The method of claim 16, wherein the DRAM comprises a memory module installed in a memory slot of the computer system.

15 Claim 19 (Original): A method for storing data in a computer system, the computer system comprising a processor for controlling operations of the computer system, a dynamic random access memory (DRAM) electrically connected to the processor for storing the data, a south bridge chipset electrically connected to the processor and the DRAM for converting a hard-disk access command into a memory access
20 command and for executing the memory access command corresponding to the hard-disk access command to access the DRAM, the method comprising:

a data maintaining method for providing a battery device to constantly self-refresh the DRAM for maintaining the data stored in the DRAM when the computer system performs a power supply management operation consistent with an
25 advanced mode and an advanced configuration and power interface (ACPI) and enters a power-saving mode.

Claim 20 (Currently Amended): The method of claim 19, wherein the computer system

40

Appl. No. 10/604,268
Amdt. dated September 30, 2005
Reply to Office action of June 30, 2005

further comprises the battery device electrically connected to the south bridge chipset for providing the operating voltage that self-refreshes the DRAM.

Claim 21 (Original): The method of claim 19, wherein the computer system further
5   comprises a switch electrically connected to the battery device wherein when the computer system enters the power-saving mode, the power supply ceases providing the operating voltage for self-refreshing the DRAM, and the switch will be enabled to make the battery device provide the operating voltage for self-refreshing the DRAM.
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Claim 22 (Currently Amended): The method of claim 21, wherein the power-saving mode comprises [[a]] an S4 status.

Claim 23 (Currently Amended): The method of claim 21, wherein the power-saving mode comprises [[a]] an S5 status.

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41